ENGLISH TRANSLATION OF INTERNATIONAL APPLICATION AS FILED

DESCRIPTION

MULTILAYER SUBSTRATE WITH BUILT-IN CHIP-TYPE ELECTRONIC COMPONENT AND METHOD FOR MANUFACTURING THE SAME

Technical Field

The present invention relates to a multilayer substrate with a built-in chip-type electronic component and a method for manufacturing the same.

Background Art

As this type of conventional technique, Patent Document 1 discloses a multilayer ceramic substrate and a method for manufacturing the same. In the multilayer ceramic substrate and the method for manufacturing the same disclosed in Patent Document 1, ceramic functional elements such as a capacitor element, an inductor element, a resistor element, and the like are previously formed using a sintered plate prepared by firing, and each of these functional elements is connected to an internal conductor film and via hole conductor and build in a green composite laminate. The green composite laminate includes a green substrate layer, a constrained layer containing a hardly sinterable material, and a wiring conductor. When the green composite laminate is fired, shrinkage of the green substrate layer in the direction of a main surface is suppressed by the constrained layer. In this technique, firing is performed by a nonshrinkage step using the constrained layer, and thus the green composite laminate with the built-in functional elements can be fired with no problem while maintaining the characteristics of the functional elements after firing because of no mutual diffusion of the constituents between the functional elements composed of the sintered plate and the green substrate layer.

In the multilayer ceramic substrate disclosed in Patent Document 1, in order to provide the sintered plate built in the ceramic multilayer substrate, the sintered plate is bonded to a conductor pattern of an internal conductor film and the like, which are formed on a ceramic green sheet using conductive paste, and then another ceramic green sheet is laminated, followed by pressure-bonding to form a ceramic green laminate.

Patent Document 1: Japanese Unexamined Patent Application Publication No. 2002-084067

Disclosure of Invention

Problem to be Solved by the Invention

In the conventional technique disclosed in Patent Document 1, when a positional shift occurs due to poor alignment between the sintered plate and the internal conductor film, thereby causing a slight connection between the sintered plate and the internal conductor film, a defect possibly occurs in a connection to the sintered plate.

On the other hand, when a surface-mounted component is mounted on a surface electrode on a substrate by soldering, self-alignment of the surface-mounted component is caused during reflow, and thus the above-described problem does not occur. However, when the built-in sintered plate is provided, a self-alignment function is not performed, and thus a positional shift due to poor alignment of the sintered plate cannot be corrected because the mounting precision is directly reflected. Therefore, in forming the built-in sintered plate, connection reliability cannot be obtained unless a connection part (electrode pad) between the internal conductor film and the sintered plate is larger than a surface electrode on the substrate. Also, the wiring density is decreased by providing a larger electrode pad

on the internal conductor film, thereby causing the problem of failing to decease the size of the ceramic multilayer substrate.

The present invention has been achieved for solving the above-described problems, and an object of the invention is to provide a multilayer substrate having a built-in chip-type electronic component, which is capable of significantly increasing the connection reliability between the built-in chip-type electronic component and an internal conductor, and a method for manufacturing the same.

Means for Solving the Problem

A multilayer substrate with a built-in chip-type electronic component according to claim 1 of the present invention includes a laminate containing a plurality of dielectric layers, a chip-type electronic component buried in the laminate and having a terminal electrode, and a via conductor provided in the dielectric layers in the lamination direction, wherein the terminal electrode of the chip-type electronic component is connected to at least one of the upper and lower end surfaces of the via conductor, and a connection step is formed in the via conductor.

According to claim 2 of the present invention, in the multilayer substrate with the built-in chip-type electronic component according to claim 1, the dielectric layers are ceramic layers, the laminate is a ceramic laminate including a plurality of the ceramic layers, and the chip-type electronic component includes a ceramic sintered body used as an element body.

According to claim 3 of the present invention, in the multilayer substrate with the built-in chip-type electronic component according to claim 2, the ceramic layers are composed of a low-temperature co-fired ceramic material, and the via conductor is composed of a conductor material containing silver or copper as a main constituent.

A method for manufacturing a multilayer substrate with a built-in chip-type electronic component according to claim 4 includes the steps of disposing a chip-type electronic component having a terminal electrode on a dielectric layer having a via conductor so that the terminal electrode comes in contact with the via conductor, and laminating the dielectric layer having the chip-type electronic component disposed thereon and another dielectric layer to form a laminate having the built-in chip-type electronic component.

According to claim 5 of the present invention, in the method for manufacturing the multilayer substrate with the built-in chip-type electronic component according to claim 4, each of the dielectric layers includes a ceramic green body, the chip-type electronic component includes a ceramic sintered body used as an element body, and the ceramic green body having the chip-type electronic component disposed thereon and the other ceramic green body are laminated to form a ceramic green laminate having the built-in chip-type electronic component, followed by firing of the ceramic green laminate.

According to claim 6 of the present invention, in the method for manufacturing the multilayer substrate with the built-in chip-type electronic component according to claim 5, the other ceramic green body has a via conductor to be connected to the terminal electrode of the chip-type electronic component.

According to claim 7 of the present invention, the method for manufacturing the multilayer substrate with the built-in chip-type electronic component according to claim 5 or 6 further includes the steps of forming the ceramic green bodies using a low-temperature co-fired ceramic material, and forming a conductor pattern composed of silver or copper as a main constituent in the ceramic green laminate.

According to claim 8 of the present invention, the method

for manufacturing the multilayer substrate with the built-in chip-type electronic component according to any one of claims 5 to 7 further includes the step of adding a shrinkage suppression layer composed of a hardly sinterable powder, which is not substantially sintered at the sintering temperature of the ceramic green bodies, in the ceramic green laminate or on a surface thereof.

Advantage of the Invention

According to claims 1 to 8 of the present invention, the present invention can provide a multilayer substrate with a built-in chip-type electronic component and a method for manufacturing the same, which are capable of significantly improving the connection reliability between the built-in chip-type electronic component and an internal conductor.

Brief Description of the Drawings

Figs. 1(a) to (c) are views showing a ceramic multilayer substrate with a built-in chip-type electronic component according to an embodiment of the present invention, in which Fig. 1(a) is a sectional view showing the whole, Fig. 1(b) is an enlarged sectional view showing a principal portion, and Fig. 1(c) is a plan view of the principal portion shown in Fig. 1(b).

Figs. 2(a) and (b) are plane views each showing a principal portion of a multilayer substrate with a built-in chip-type electronic component according to another embodiment of the present invention, the plane views corresponding to Fig. 1(c).

Figs. 3(a) to (c) are views each showing a principal portion in a step for manufacturing the ceramic multilayer substrate shown in Figs. 1, in which Fig. 3(a) is a sectional view showing a ceramic green sheet, Fig. 3(b) is a sectional view showing a state in which chip-type electronic components are mounted on the

ceramic green sheet shown in Fig. 3(a), and Fig. 3(c) is a sectional view showing a state in which the ceramic green sheet shown in Fig. 3(b) and other ceramic green sheets are laminated.

Fig. 4(a) to (c) are views each showing a step after the manufacturing steps shown in Figs. 2, in which Fig. 4(a) is a sectional view showing a press-bonded body before firing, Fig. 4(b) is a sectional view showing the ceramic multilayer substrate after firing, and Fig. 4(c) is a sectional view showing a state in which chip-type electronic components are mounted on the ceramic multilayer substrate shown in Fig. 4(b).

Fig. 5(a) and (b) are sectional views each illustrating a shift of the mounting position of a chip-type electronic component of the ceramic multilayer substrate shown in Figs. 1, in which Fig. 5(a) is a sectional view illustrating a state in which no positional shift occurs, and Fig. 5(b) is a sectional view illustrating a state in which a positional shift occurs.

Fig. 6 is an enlarged sectional view showing a principal portion of a multilayer substrate with a built-in chip-type electronic component according to a further embodiment of the present invention.

Reference Numerals

10 ceramic multilayer substrate (multilayer substrate)

11 ceramic laminate (laminate)

11A ceramic layer (dielectric layer)

12 internal conductor pattern

12B via conductor

12C connection step

13, 113 chip-type electronic component

13A, 113A external terminal electrode (terminal electrode)

111 ceramic green laminate

111A ceramic green sheet (ceramic green body)

116 constrained layer (shrinkage suppression layer)

Best Mode for Carrying Out the Invention

The present invention will be described on the basis of embodiments shown in Figs. 1 to 6.

For example, as shown in Fig. 1(a), a multilayer substrate 10 having a built-in chip-type electronic component according to an embodiment is a ceramic multilayer substrate including a ceramic laminate in which a plurality of ceramic layers 11A is laminated, and internal conductor patterns 12 are formed, and a plurality of chip-type electronic components 13 disposed at an interface between the upper and lower ceramic layers 11A, the chip-type electronic components 13 each including a ceramic sintered body as an element body and external terminal electrodes 13A formed at both ends thereof. Also, surface electrodes 14 are formed on both main surfaces (upper and lower surfaces) of the ceramic laminate 11. Therefore, in description below, the multilayer substrate 10 with the built-in chip-type electronic component is referred to as the "ceramic multilayer substrate 10" hereinafter.

As shown in Fig. 1(a), a plurality of surface-mounted components 20 is mounted on the upper surface of the ceramic laminate 11 through the surface electrodes 14. As the surface-mounted components 20, active elements such as a semiconductor element, a gallium arsenic semiconductor element, and the like, passive elements such as a capacitor, an inductor, a resistor, and the like, etc. are electrically connected to the surface electrodes 14 on the upper surface of the ceramic laminate 11 through solder, a conductive resin, or a bonding wire of Au, Al, Cu, or the like. The chip-type electronic components 13 are electrically connected to the surface-mounted components 20 through the surface electrodes 14 and the internal conductor

patterns 12. The ceramic multilayer substrate 10 can be mounted on a mount substrate such as a mother board or the like through the surface electrodes 14 formed on the lower surface.

The material of the ceramic layers 11A constituting the ceramic laminate 11 is not particularly limited as long as it is a ceramic material. In particular, a low temperature co-fired ceramic (LTCC) material is preferred. The low temperature co-fired ceramic material is a ceramic material which can be sintered at a temperature of 1050°C or less and co-sintered with silver or copper having low resistivity. Examples of the low temperature co-fired ceramic material include glass composite LTCC materials each including a mixture of a ceramic powder of alumina or forsterite and borosilicate glass; crystallized glass LTCC materials each including ZnO-MaO-Al_2O_3-SiO_2 crystallized glass; and non-glass LTCC materials each including a BaO-Al_2O_3-SiO ceramic powder or Al_2O_3-CaO-SiO_2-MgO-B_2O_3 ceramic powder.

By using the low temperature co-fired ceramic material as the material for the ceramic laminate 11, a metal having low resistance and low melting point, such as Ag or Cu, can be used for the internal conductor patterns 12 and the surface electrodes 14, and thus the ceramic laminate 11 and the internal conductor patterns 12 can be co-fired at a low temperature of 1050°C or less.

As the ceramic material, a high temperature co-fired ceramic material (HTCC) material can be used. An example usable as the high temperature co-fired ceramic material is prepared by sintering a mixture of alumina, aluminum nitride, mullite, or the like and a sintering aid, such as glass, at 1100°C or more. In this case, a metal selected from molybdenum, platinum, palladium, tungsten, nickel, and alloys thereof can be used for the internal conductor patterns 12 and the surface electrodes 14.

As shown in Fig. 1(a), the ceramic laminate 11 has the

internal conductor patterns 12 formed therein and the surface electrodes 14 formed on the upper and lower surfaces. Each of the internal conductor patterns 12 includes a planar conductor 12A formed in a predetermined pattern along an interface between the upper and lower ceramic layers 11A, and a via conductor 12B formed in, for example, a cylindrical shape, so as to pass in a predetermined pattern through the corresponding ceramic layer 11A in the lamination direction thereof so that the upper and lower planar conductors 12A are connected to each other.

As shown in Figs. 1(a) and (b), the chip-type electronic components 13 are disposed on one of the interfaces between the upper and lower ceramic layers 11A, and each of the external terminal electrodes 13A is connected directly to at least one of the upper and lower end surfaces of the via conductors 12B. The chip-type electronic components 13 are connected to the via conductors 12B through a plurality of connection patterns. Namely, in this embodiment, the chip-type electronic components 13 are connected to the via conductors 12B through three connection patterns X, Y, and Z as shown by circles in Fig. 1(a).

First, the connection pattern X will be described with reference to Figs. 1(b) and (c). As shown in Figs. 1(a) to (c), a pair of the right and left external terminal electrodes 13A of the corresponding chip-type electronic component 13 is connected to a pair of the right and left via conductors 12B formed in the ceramic layer 11A in contact with the lower surface of the chip-type electronic component 13. Furthermore, opposing steps (referred to as "connection steps" hereinafter) 12C are formed in the respective upper end surfaces of the pair of via conductors 12B so that the external terminal electrodes 13A are closely connected to the respective connection steps 12C. Each of the connection steps 12C is formed by cutting out a half of the upper end surface of the via conductor 12B and has a L-shaped sectional

form. Therefore, a substantially lower half of each external terminal electrode 13A of the chip-type electronic component 13 is connected to the via conductor 12B through the two surfaces including the vertical surface and the bottom surface of each of the opposing connection steps 12C. In other words, the rectangular chip-type electronic component 13 is connected to the corresponding via conductors 12B through at least two surfaces each, i.e., the end surface and the bottom. In Fig. 1(b), a monolithic ceramic capacitor is shown as a chip-type electronic component 13 including ceramic sintered body 13B used as an element body and internal electrodes 13C.

In the connection pattern Y, one (the right in Fig. 1(a)) of the corresponding external terminal electrodes 13A of the chip-type electronic component 13 is connected to the connection step 12C of the via conductor 12B formed in the lower ceramic layer 11A, and the other external terminal electrode 13A (the left in Fig. 1(a)) is connected to the connection step 12C of the via conductor 12B formed in the upper ceramic layer 11A. In this case, the right via conductor 12B is formed in the same shape as that of the right via conductor 12B shown in Fig. 1(b). The left via conductor 12B has the connection step 12C formed at the lower end thereof. The connection steps 12C of the right and left via conductors 12B have opposing planes of connection to the respective external terminal electrodes 13A and also have a positional relation in which the rotation angle between the steps around the chip-type electronic component 13 is 180°. In this connection pattern, the via conductors 12B connected to the respective external terminal electrodes 13A are separated, and thus the pitch between the via conductors 12B can be narrowed, thereby complying with reduction in size of the chip-type electronic components 13 and sufficiently securing isolation between the respective via conductors 12B.

In the connection pattern Z, one (the right in Fig. 1(a)) of the external terminal electrodes 13A of the corresponding chip-type electronic component 13 is connected to the connection step 12C of the via conductor 12B formed in the lower ceramic layer 11A, and the other external terminal electrode 13A (the left in Fig. 1(a)) is connected to the upper and lower connection steps 12C of the via conductors 12B continuously formed in the upper and lower ceramic layers 11A, respectively, so that the external terminal electrode 13A is held between the upper and lower connection steps 12C. In this case, the right via conductor 12B is formed in the same shape as that of the right via conductor 12B in the connection pattern X. Among the left via conductors 12B, the lower via conductor 12B is formed in the same shape as that of the left via conductor 12B in the connection pattern X, and the upper via conductor 12C is formed in the same shape as that of the lift via conductor 12C in the connection pattern Y. In this connection pattern, the reliability of connection between the external terminal electrodes 13A and the via conductors 12B can be further improved.

The via conductors 12B to which each chip-type electronic component 13 is connected are not limited to those shown in Figs. 1(a) to (c), and, for example, the via conductors shown in Figs. 2(a) and (b) may be used.

The via conductors 12'B shown in Fig. 2(a) are formed to have an elliptic planar shape in which the long axis is slightly longer than the width of the chip-type electronic component 13. The external terminal electrodes 13A of the chip-type electronic component 13 are disposed so that the end surfaces coincide with the long axes of the respective via conductors 12'B, and closely connected to the connection steps 12'C formed in the upper surfaces of the respective via conductors 12'B. As estimated from Fig. 2(a), each of the connection steps 12'C has three

vertical wall surfaces and a bottom surface corresponding to the end surface, both side surfaces, and the bottom surface of the corresponding external terminal electrode 13A so that each connection step 12'C is connected to the corresponding external terminal electrode 13A through the four surfaces. Like in the case shown in Figs. 1, the three vertical wall surfaces are connected to a substantially lower half of each external terminal electrode 13A. Therefore, the area of contact of each via conductor 12'B with the corresponding external terminal electrode 13A is larger than that shown in Figs. 1, thereby further increasing connection reliability.

The via conductors 12"B shown in Fig. 2(b) are formed in the same circular shape as that of the via conductors shown in Figs. 1, but the outer diameter thereof is slightly smaller than that shown in Figs. 1. One of the external terminal electrodes 13A of the chip-type electronic component 13 is closely connected to connection steps 12"C formed in two via conductors 12"B disposed with a space therebetween. The two via conductors 12"B are disposed so that a line passing through the centers thereof substantially coincides with the end surface of each external terminal electrode 13A of the chip-type electronic component 13, and the two via conductors 12"B are symmetric with respect to the axis of the chip-type electronic component 13. As estimated from Fig. 2(b), the connection step 12"C of one of the two via conductors 12"B has two vertical wall surfaces and a bottom surface corresponding to the end surface, one of the side surfaces, and the bottom surface of each external terminal electrode 13A so that the connection step 12"C is connected to a half of the end of each external terminal electrode 13A through the three surfaces. Similarly, the other via conductor 12"B is connected to the remaining half of the end of each external terminal electrode 13A through the three surfaces. Therefore,

the via conductors 12"B are connected to each external terminal electrode 13A in a contact area which is middle between the case shown in Figs. 1 and the case shown in Fig. 2(a), thereby increasing connection reliability.

Examples of the chip-type electronic components 13 include, but are not particularly limited to, components each including, as an element body, a ceramic sintered body formed by firing barium titanate, ferrite, or the like at 1200°C or more. Specific examples of such components include chip-type electronic components such as an inductor, a filter, a balun, a coupler, and the like, in addition to the monolithic ceramic capacitor shown in Fig. 1(b). These chip-type electronic components can be used alone or in combination of two or more appropriately selected from these. In the case shown in Fig. 1(a), a plurality of the chip-type electronic components 13 is disposed on the same ceramic layer 11A. However, the chip-type electronic components 13 may be disposed at any desired interfaces between the upper and lower ceramic layers 11A according to demand. Alternatively, a plurality of the chip-type electronic components 13 may be laminated over a plurality of different interfaces in the vertical direction. The plurality of chip-type electronic components 13 may be connected in series and/or parallel through the connection steps 12C of the via conductors 12B to realize increases in functionality and performance of the ceramic multilayer substrate 10 according to purposes.

Next, a method for manufacturing the ceramic multilayer substrate 10 will be described with reference to Figs. 3 to 5.

In this embodiment, manufacture of the ceramic multilayer substrate 10 using a nonshrinkage method is described. The term "nonshrinkage method" means a method in which when a ceramic material is used for the ceramic laminate 11, the ceramic laminate causes substantially no dimensional change in the planar

direction during firing.

In this embodiment, first, a plurality of ceramic green sheets is prepared using slurry containing, for example, a low temperature co-fired ceramic material. Also, as shown in Figs. 3(a) and (b), via holes are formed in a predetermined pattern in a ceramic green sheet 111A, for mounting chip-type electronic components 113 each including a ceramic sintered body used as an element body. These via holes are preferably formed as circular through holes each having a diameter slightly smaller than the width of the chip-type electronic components 113 and larger than the diameter of via conductors formed in other ceramic green sheets. The via holes are filled with conductive paste containing, for example, Ag or Cu, as a main constituent, to form via conductor parts 112B. Furthermore, the same conductive paste is applied in a predetermined pattern on another ceramic green sheet 111A by screen printing to form surface electrode parts 114 (refer to Fig. 3(c)). In the ceramic green sheet 111A, the surface electrode parts 114 are appropriately connected to the via conductor parts 112B. Other ceramic green sheets 111A each having in-plane conductor parts 112A and/or the via conductor parts 112B are prepared in the same manner as described above. The via holes may be formed as through holes for forming the via conductors 12B shown in Figs. 2(a) or (b).

In description below, the chip-type electronic components during firing are denoted by reference numeral 113, and the chip-type electronic components after firing and subsequent temperature drop are denoted by reference numeral 13.

Next, an organic adhesive is applied or sprayed, using a spray or the like, on the in-plane conductor parts 112A on the upper surface of the ceramic green sheet 111A on which the chip-type electronic components 113 to be disposed, to form organic adhesive layers (not shown). As shown in Fig. 3(b), the external

terminal electrode parts 113A of each chip-type electronic component 113 are aligned with the respective via conductor parts 112B of the ceramic green sheet 111A, and the chip-type electronic components 113 are mounted on the ceramic green sheet 111A. Then, the external terminal electrodes 113A of the chip-type electronic components 113 are bonded and fixed to the respective via conductor parts 112B through the organic adhesive layers. As the organic adhesive, a mixture containing synthetic rubber or a synthetic resin and a plasticizer can be used. The thickness of the organic adhesive layers is preferably 3 μm or less in the case of application and 1 μm or less in the case of spraying.

Then, as shown in Fig. 3(c), the ceramic green sheets 111A each having the in-plane conductor parts 112A and/or the via conductor parts 112B and the ceramic green sheet 111A having the chip-type electronic components 113 mounted thereon are laminated in a predetermined order on a constrained layer 116. Also, the uppermost ceramic green sheet 111A having the surface electrodes 114 is laminated to form a ceramic green laminate 111 on the constrained layer 116. Furthermore, another constrained layer 116 is laminated on the upper surface of the ceramic green laminate 111, and the ceramic green laminate 111 is subjected to heat-bonding under pressure at a predetermined temperature and pressure through the upper and lower constrained layers 116 to obtain a pressure-bonded body 110 shown in Fig. 4(a). As the constrained layers 116, a sheet is formed as shown in Fig. 4(a) using a paste containing a hardly sinterable powder (for example, a ceramic powder having a high sintering temperature, such as Al_2O_3 or the like) which is not sintered at the sintering temperature of the ceramic green laminate 111, e.g., Al_2O_3, as a main constituent and an organic binder as a secondary constituent.

When each of the chip-type electronic components 113 is correctly disposed at a predetermined position of the via conductor parts 112B of the corresponding ceramic green sheet 111A, as shown in Fig. 5(a), each chip-type electronic component 113 is buried in the ceramic green sheet 111A by a pressure bonding operation and connected to the light and left via conductor parts 112B through the right and left external terminal electrode parts 113A, respectively, while forming the connection steps 112C by uniform compressive deformation of inner halves of the respective upper surfaces of the light and left via conductor parts 112b. Therefore, the right and left external terminal electrode parts 113A are connected to the respective connection steps 112C through two surfaces each.

For example, when the chip-type electronic component 113 is shifted to the left from a predetermined position, as shown in Fig. 5(b), the chip-type electronic component 113 is connected to the right and left via conductor parts 112B while forming the connection steps 112C by compressive deformation of the via conductor parts 112B so that the left external terminal electrode part 113A comes in contact with the left via conductor part 112B in a larger contact area, and the right external terminal electrode part 113A comes in contact with a portion of the right via conductor part 112B in a small contact area. Namely, even when one of the external terminal electrode parts 113A comes in contact with a portion of the corresponding via conductor part 112B, the via conductor parts 11B are deformed without being cut by compressive deformation while maintaining contact with the external terminal electrode parts 113A. Therefore, as shown in Fig. 5(b), the external terminal electrode parts 113A are securely connected to the respective via conductor parts 112B.

After the pressure-bonded body 110 with the built-in chip-type electronic components 113 is formed as described above, the

pressure-bonded body 110 shown in Fig. 4(a) is fired, for example, at 870°C in an air atmosphere to obtain the ceramic multilayer substrate 10 shown in Fig. 4(b). The external terminal electrode parts 113A of each of the built-in chip-type electronic parts 113 are connected to the respective via conductor parts 112B by integration due to grain growth of the metal grains of these parts during sintering. The firing temperature is preferably the sintering temperature of a low temperature co-fired material, for example, in a range of 800°C to 1050°C. At a firing temperature lower than 800°C, the ceramic constituents of the ceramic green laminate 111 may not be sufficiently sintered, while at a temperature over 1050°C, the metal grains of the internal conductor patterns 12 may be melted and diffused into the ceramic green laminate 111.

After firing, the upper and lower constrained layers 116 are removed by blasting or ultrasonic washing to prepare the ceramic multilayer substrate 10. Furthermore, as shown in Fig. 4(c), predetermined surface-mounted components 20 are mounted on the surface electrodes 14 of the ceramic multilayer substrate 10 by soldering or the like to obtain a final product. The external terminal electrode parts 113A of the chip-type electronic components 113 may be in the form of a paste coating after baking or a dried paste coating before baking.

Furthermore, the surface-mounted components 20 are used in appropriate combination with the chip-type electronic components 13, as shown in Fig. 1(a). The chip-type electronic components 13 are connected to the surface-mounted components 20 through the surface electrodes 14 and the internal conductor patterns 12. When the surface-mounted components 20 are components susceptible to power noise, such as integrated circuits or the like, a monolithic ceramic capacitor may be connected as the chip-type electronic component 13 near a portion immediately below a power

terminal and ground terminal of each surface-mounted component 20. In this case, the terminal arrangement of the surface-mounted components 20 such as integrated circuits or the like is not limited, and chip-type electronic components (e.g., monolithic ceramic capacitors or the like) need not be separately mounted on a mother board. Therefore, a power supply voltage can be stably supplied and output oscillation can be prevented, thereby removing noise with a high efficiency.

As described above, in this embodiment, the chip-type electronic components 113 each including a ceramic sintered body used as an element body and terminal electrodes are disposed on the ceramic green sheet 111A having the via conductor parts 112B so that the external terminal electrode parts 113A of each chip-type electronic component 113 come into contact with the respective via conductor parts 112B. Then, the other ceramic green sheets 111A and the ceramic green sheet 111A having the chip-type electronic components 113 disposed thereon are laminated to form the ceramic green laminate 111 having the built-in chip-type electronic components 113. Thereafter, the ceramic green laminate 111 is fired to prepare the ceramic multilayer substrate 10. Therefore, in the resultant ceramic multilayer substrate 10, the external terminal electrodes 13A of each chip-type electronic component 13 are connected to the respective via conductors 12B, and the connection steps 12C for connection are formed at the end surfaces of the respective via conductors 12B. Since, in the ceramic multilayer substrate 10, the external terminal electrodes 13A of each chip-type electronic component 13 are connected to the connection steps 12C formed at the end surfaces of the respective via conductors 12, the respective via conductors 12B are securely connected to the external terminal electrodes 13A without disconnection, thereby significantly increasing the connection reliability.

In this embodiment, the via conductors 12B come in contact with the upper surfaces and/or lower surfaces of the right and left external terminal electrodes 13A of each chip-type electronic component 13. Therefore, the chip-type electronic components 13 can be connected to the via conductors 12B through various connection patterns, thereby increasing the degree of freedom of the internal conductor patterns 12. Furthermore, in this embodiment, the ceramic layers 11A are low-temperature sintered ceramic layers, and thus a low-resistance inexpensive metal such as Ag or Cu can be used for the internal conductor patterns 12 and the surface electrodes 14. This can contribute to a reduction in manufacturing cost.

In this embodiment, description is made of a ceramic multilayer substrate including a ceramic laminate in which dielectric layers used as ceramic layers are laminated, and chip-type ceramic electronic components each including a ceramic sintered body as an element body are provided. However, a resin multilayer substrate may be used, in which chip-type electronic components each including a ceramic sintered body or a resin as an element body are provided in a resin laminate of resin layers used as dielectric layers.

Although, in this embodiment, description is made of a case in which the constrained layers 116 are disposed on both the upper and lower surfaces of the ceramic green laminate 111 to prepare the ceramic multilayer substrate 10. However, the constrained layers (shrinkage suppression layer) may be appropriately interposed between the ceramic green sheets in the ceramic green laminate. In this case, the shrinkage suppression layers remain in the ceramic multilayer substrate. However, the glass constituents of the ceramic green sheets are mixed in the shrinkage suppression layers during sintering of the ceramic green sheets, and thus the green ceramic material of the

shrinkage suppression layers is bonded and consolidated by the glass constituents to leave the shrinkage suppression layers as ceramic layers.

Examples

Example 1

In this example, a ceramic multilayer substrate was formed by nonshrinkage firing, and disconnection between a chip-type electronic component (monolithic ceramic capacitor) and via conductors was examined.

[Preparation of ceramic multilayer substrate]

In order to form a ceramic multilayer substrate, a slurry was prepared using Al_2O_3 serving as a filler, and a low temperature co-fired ceramic material as a ceramic material, which contained borosilicate glass serving as a sintering aid. The slurry was applied on a plurality of carrier films to prepare a plurality of ceramic green sheets. Then, via holes of 0.3 mm in diameter were formed in one of the ceramic green sheets by layer processing, and the ceramic green sheet was brought into close contact with a smooth support base. In this state, a conductive paste containing an Ag powder as a main constituent was stuffed into the via holes using a metal mask to form via conductor parts. Also, in-plane conductor parts were formed in a predetermined pattern on the ceramic green sheet by screen printing of the same conductive paste. Similarly, the via conductor parts and in-plane conductor parts were formed on the other ceramic green sheets.

Next, a monolithic ceramic capacitor was prepared as a chip-type electronic component including a sintered ceramic body as an element body. The monolithic ceramic capacitor had the sintered ceramic body (size: 0.6 mm × 0.3 mm × 0.3 mm, internal electrode:

Pd, capacity specification: 80 pF) prepared by firing at 1300°C. The monolithic ceramic capacitor also had external terminal electrode parts which were formed on both ends by applying conductive paste containing Ag as a main constituent and then baking the paste. The external terminal electrode parts were not subjected to plating. The width of the monolithic ceramic capacitor was the same as the diameter of the via conductor parts. Then, an organic adhesive was applied on a predetermined ceramic green sheet using, for example, a spray to form organic adhesive layers on the in-plane conductor parts. Thereafter, the monolithic ceramic capacitor was mounted on the ceramic green sheet using a mounter in alignment with the predetermined in-plane conductor parts and then bonded and fixed.

In this embodiment, ten ceramic green sheets of 200 mm × 200 mm square and 50 μm in thickness after firing were laminated, and a plurality of monolithic ceramic capacitors was provided so as to be located 100 μm lower a surface of the substrate after firing. As a result, a ceramic green laminate was produced.

Furthermore, sheets serving as constrained layers were laminated on both surfaces of the ceramic green laminate of 200 mm × 200 mm square, and then the laminate was subjected to preliminary pressure bonding, for example, at 10 MPa. After the preliminary pressure bonding, the laminate was subjected to primary pressure bonding, for example, at 100 MPa. In the primary pressure bonding, connection steps for connection were formed in the respective via conductor parts by the monolithic ceramic capacitors in the ceramic green laminate. After the primary pressure bonding, the pressure-bonded body was fired at 870°C in an air atmosphere, and then the green constrained layers were removed to obtain the ceramic multilayer substrate of 0.5 mm in thickness.

In Comparative Example 1, a ceramic multilayer substrate was prepared in the same manner as in Example 1 except that an electrode pad of 0.3 mm in diameter was formed on an in-plane conductor serving as a connection part for each monolithic ceramic capacitor.

[Evaluation of ceramic multilayer substrate]

Each of the ceramic multilayer substrates of Example 1 and Comparative Example 1 was cut along a line passing through the center of each of the via conductors or the electrode pads, and connections between the external terminal electrodes and the via conductors or the electrode pads were observed with SEM (scanning electron microscope). As a result, in the ceramic multilayer substrate of Example 1, a connection state, for example, shown in Figs. 5(a) or (b) was observed. It was thus found that even if a monolithic ceramic capacitor is slightly shifted from the position of a corresponding via conductor, the monolithic ceramic capacitor is connected to the via conductor without disconnection, as shown in Fig. 5(b).

On the other hand, in Comparative Example 1, some of the monolithic ceramic capacitors were shifted from the positions of the corresponding electrode pads, thereby cutting the electrode pads by the monolithic ceramic capacitors.

Therefore, it was found that when an external terminal electrode is connected to a via conductor through a connection step, both can be securely connected to each other, thereby significantly increasing connection reliability. In this example, when a ceramic green sheet was locally deformed on the order of several tens μm by burying a monolithic ceramic capacitor, wiring with printed electrodes was easily cut because the thickness of the electrodes was several μm. However, the via conductors were not cut because the via conductors had a cylindrical shape having

a thickness equivalent to the sheet thickness.

Example 2

In this embodiment, a ceramic multilayer substrate was formed in the same manner using the same materials as in Example 1. However, in this embodiment, the built-in monolithic ceramic capacitor used had a sintered ceramic body (size: 1.6 mm×0.8 mm×0.5 mm, internal electrode: Ni, capacity specification: 1 μF) and external terminal electrode parts which were formed on both ends by applying a conductive paste containing Ag as a main constituent and then baking the paste. As shown in Fig. 6, an integrated circuit element (IC) was disposed as a surface-mounted component 20 on the upper surface of the ceramic multilayer substrate 10, and a monolithic ceramic capacitor 13 was disposed as a bypass capacitor immediately below the IC. One of external terminal electrodes 13A of the monolithic ceramic capacitor 13 was connected directly to a power supply of the IC through a via conductor 12B, and the other external terminal electrode 13A of the monolithic ceramic capacitor 13 was connected, through a via conductor 12B, to an in-plane conductor 12A formed as a ground layer in the ceramic multilayer substrate 10. The external terminal electrodes 13A of the monolithic ceramic capacitor 13 were connected to the respective via conductors 12B through connection steps 12C.

Since a bypass capacitor is generally inevitably disposed outside an IC on a substrate, connection to the bypass capacitor on the substrate is achieved by extending wiring from the inside of the substrate. In this example, the IC is connected directly to the monolithic ceramic capacitor 13 serving as a bypass capacitor through the via conductors 12B, and thus the impedance between both can be decreased as much as possible. In addition,

the external terminal electrodes 13A of the monolithic ceramic capacitor 13 are connected to the respective via conductors 12B through the connections steps 12C, thereby increasing the connection reliability.

Example 3

In this example, the amount of the sintering aid added to a low temperature co-fired ceramic material to be added to a constrained layer was changed to change the adhesive force of the constrained layer to a laminate of ceramic green sheets. A ceramic multilayer substrate was formed in the same manner as in Example 1 except that the amount of shrinkage in a planar direction of the laminate was controlled as shown in Table 1.

Next, the occurrence of cracks in the ceramic multilayer substrate and the monolithic ceramic capacitors was observed by X-ray crack detection. As a result, as shown in Table 1, when an amount of shrinkage of the ceramic laminate increased to the minus side beyond -5%, cracks were detected in the built-in monolithic ceramic capacitor, while when an amount of shrinkage of the ceramic laminate increased to the plus side beyond +5%, cracks were detected in both the built-in monolithic ceramic capacitors and the ceramic laminate.

[Table 1]

Conte of sintering aid (% by weight)	Amount of shrinkage (%)	Influence on component and substrate	Number of cracked components in 200 mm substrate (/400 components)
1.7	-5.1	Cracks in component	241
1.6	-5.0	No problem	0
1.4	-4.0	No problem	0
1.2	-2.0	No problem	0
1.0	-1.0	No problem	0
0.5	0	No problem	0
0.3	+1.0	No problem	0
0.2	+3.0	No problem	0
0.1	+5.0	No problem	0
0.0	+5.1	Cracks in substrate and component	165

The results shown in Table 1 indicate that when an amount of shrinkage of the ceramic layers exceeds ±5%, cracks occur in the monolithic ceramic capacitors and/or the ceramic laminate even if the monolithic ceramic capacitors are connected to the via conductors without disconnection. It is thus found that the amount of the sintering aid added to a constrained layer is preferably determined to 0.1% by weight to 1.6% by weight which shows an amount of shrinkage in a range of ±5%.

The present invention is not limited to the above-described embodiments and includes any embodiment within the scope of the gist of the invention.

Industrial Applicability

The present invention can be preferably applied to a ceramic

multilayer substrate and a method for manufacturing the same used for electronic devices and the like.